MWμL
PLANAR EPITAXIAL MILLIWATT MICROLOGIC® INTEGRATED CIRCUITS

WHAT IS MILLIWATT MICROLOGIC?

The Fairchild Milliwatt Micrologic (MWμL) elements are a set of compatible, integrated logic building blocks. The elements are manufactured using the Fairchild PLANAR Epitaxial Process by which all the necessary transistors and resistors are diffused into a single silicon wafer. The individual RTL gates within the logic blocks are interconnected by metal over oxide.

SPEED AND POWER

Epitaxial Milliwatt Micrologic is characterized by very low propagation delays at low DC power dissipation. Typical propagation delay for the basic RTL circuit is 40 nanoseconds and its power dissipation is typically 2 mW.

ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature)

Maximum voltage applied to pin 8 (continuous)	8 V
Maximum voltage applied to any input pin	±4.0 volts
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation	250 mW
Maximum Voltage applied to pin 8 (Pulsed, ≤1 second)	12 V

PURCHASING INFORMATION

Purchasing Agent please note:

To order part, the following numbering system should be used to expedite handling. The complete number will be a seven digit number with the designations as follows.

ABCDEFG

A = 9 for all elements.

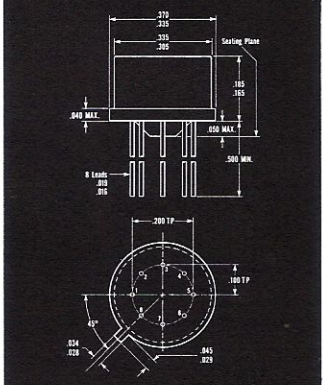
B = 5 for the TO-5 package. 1 for the flat package.

CDE = the three digit number denoting the specific element desired (i.e. the buffer) would be 909.

F = 2 for planar epitaxial material.

G = 1 for −55°C to +125°C operation.

PHYSICAL DIMENSIONS
(SIMILAR TO TO-5)



NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated kovar
Weight: 1.12 grams

AMBIENT TEMPERATURE OPERATION

The Milliwatt Micrologic elements may be used in accordance with the Loading Chart below through the full military temperature range of −55°C to +125°C. Nominal Supply voltage is 3.00 Volts. The Loading Chart below is valid for V_{CC} = 3.00 Volts ±10%. Improved speed and Noise Immunity will result if V_{CC} is increased above 3.00 Volts to a maximum of 3.66 Volts at +125°C with maximum V_{CC} increasing linearly to 4.5 Volts at −55°C.

ELEMENTS

The 908 Element (ADDER) performs MOD 2 Addition, the exclusive OR function, and control of 2 data streams (pins 1 and 5) by tying pins 2 and 3 together to control.

The 909 Element (BUFFER) is a 2 input, high fan-out, inverting gate, with internal timing resistor.

The 910 Element (DUAL GATE) is a dual, 2 input gate.

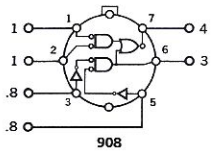
The 911 Element (GATE) is a 4 input gate with added inverter for the output to generate OR, NOR, AND, and NAND functions.

The 912 Element (HALF-ADDER) is a two-level AND-OR gate with added output inverter.

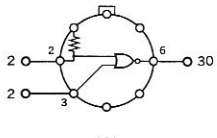
The 913 Element (TYPE D FLIP-FLOP) is a gated D-Flip-Flop with asynchronous set and reset inputs suitable for shifting and counting. The 913 was previously known as an R, Register, or Full Shift Register Element.

The 921 Element (EXPANDER) is a dual 2 input gate without node resistors, to be used when increased fan-in is required.

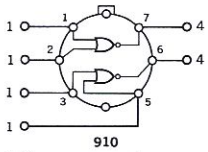
MWμL LOADING CHART valid for system operation from −55°C to +125°C (symbols shown top view)



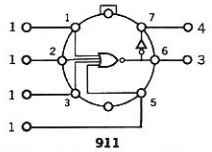
908



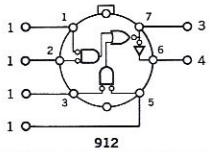
909



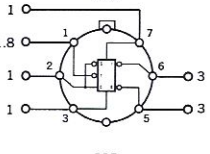
910



911



912



913

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

COPYRIGHT FAIRCHILD SEMICONDUCTOR, 1966 • PRINTED IN U.S.A. 2320-125-46 10M

MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3025589, 3064167, 3108359, 3117260. OTHER PATENTS PENDING.

GENERAL RULES

The number of elements that may be driven by an output terminal may consist of any combination of elements whose summation of input loading does not exceed the output terminal driving capability.

Unused input pins should be tied to ground.

See expander element (921) for paralleling.

FIG. 1
TYPICAL POWER DISSIPATION VS. V_{CC}

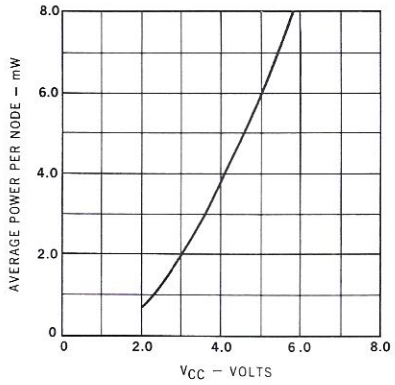


FIG. 2a
TYPICAL SIGNAL LEVEL VS. TEMPERATURE
V_{CC} = 3.0V

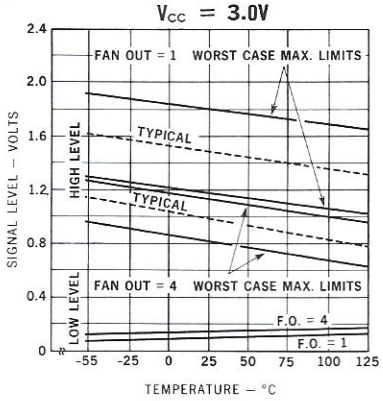


FIG. 2b
TYPICAL SIGNAL LEVEL VS. TEMPERATURE
V_{CC} = 4.0V

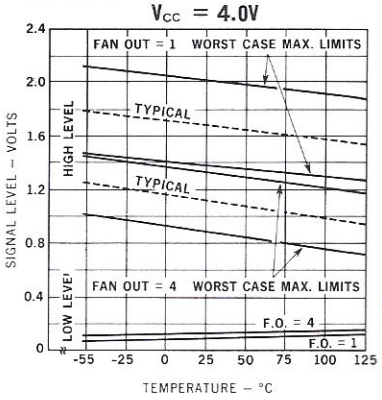
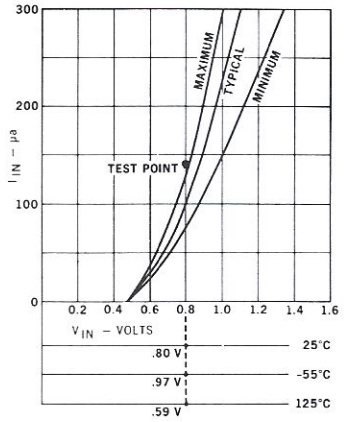
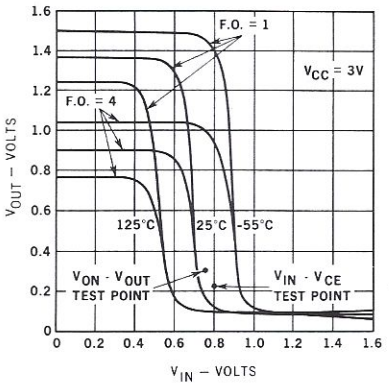


FIG. 3
TYPICAL INPUT CHARACTERISTICS



Note: This curve will apply as V_{CC} is increased from 3 V to 5 V with small decrease in I_{IN} for same V_{IN}.

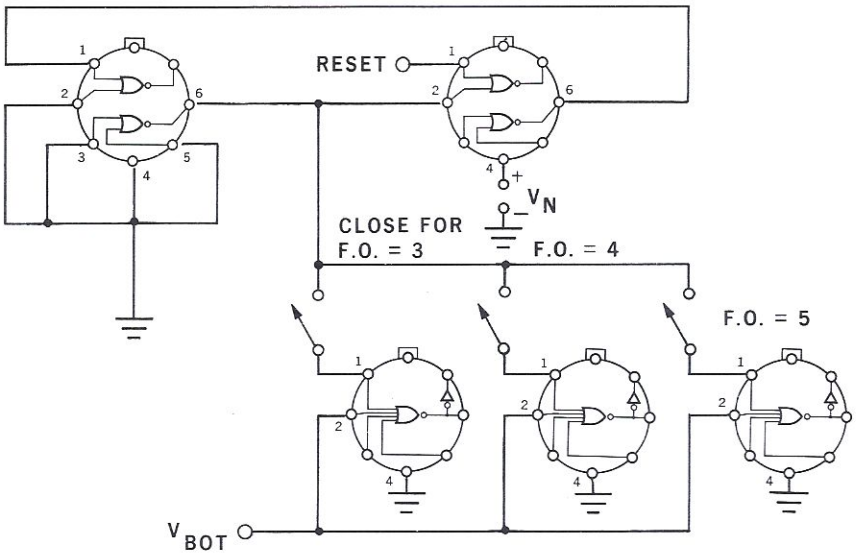
FIG. 4
TRANSFER CHARACTERISTICS



TYPICAL V_{ON} VS. V_{CC}

	–55°C	+25°C	+125°C
$V_{CC} = 3$ V	.890	.680	.530
$V_{CC} = 4$ V	.940	.710	.550
$V_{CC} = 5$ V	.990	.750	.575

FIG. 5 TEST CIRCUIT FOR NOISE THRESHOLD MEASUREMENTS



V_{CC}	V_{BOT}
3 V	1.8 V
4 V	2.0 V
5 V	2.4 V
6 V	2.9 V

Note that elements with specified fan-out = 4 have good immunity to worst case ground noise in a test circuit when used in a fan-out = 5 configuration.

FIG. 6
DC NOISE THRESHOLD VS. V_{CC}

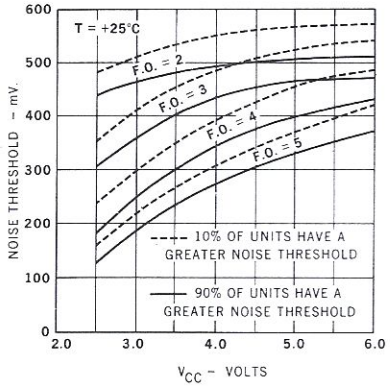

T = +25°C
F.O. = 2
F.O. = 3
F.O. = 4
F.O. = 5
10% OF UNITS HAVE A GREATER NOISE THRESHOLD
90% OF UNITS HAVE A GREATER NOISE THRESHOLD
NOISE THRESHOLD – mV
V_{CC} – VOLTS

FIG. 7
DC NOISE THRESHOLD VS. V_{CC}

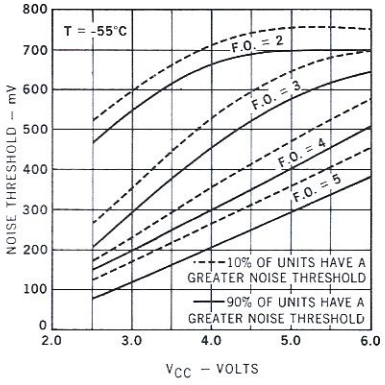

T = -55°C
F.O. = 2
F.O. = 3
F.O. = 4
F.O. = 5
10% OF UNITS HAVE A GREATER NOISE THRESHOLD
90% OF UNITS HAVE A GREATER NOISE THRESHOLD
NOISE THRESHOLD – mV
V_{CC} – VOLTS

FIG. 8
DC NOISE THRESHOLD VS. V_{CC}

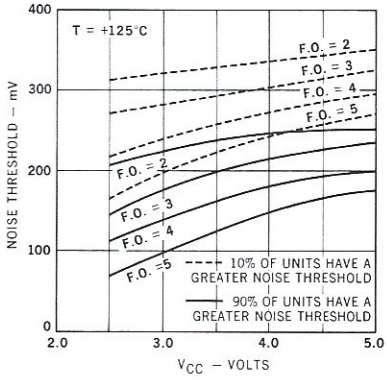

T = +125°C
F.O. = 2
F.O. = 3
F.O. = 4
F.O. = 5
10% OF UNITS HAVE A GREATER NOISE THRESHOLD
90% OF UNITS HAVE A GREATER NOISE THRESHOLD
NOISE THRESHOLD – mV
V_{CC} – VOLTS

FIG. 9
TYPICAL PULSED NOISE THRESHOLD VERSUS PULSE WIDTH

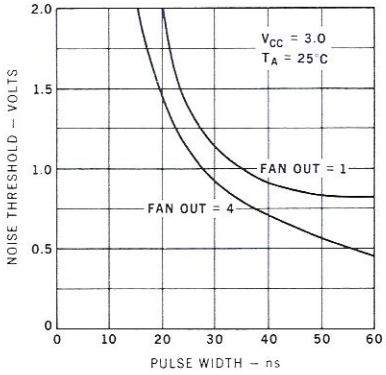


FIG. 10
TYPICAL PULSED NOISE THRESHOLD VERSUS PULSE WIDTH

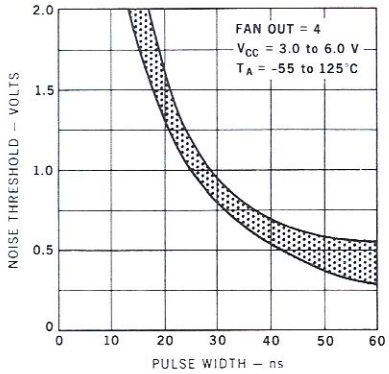
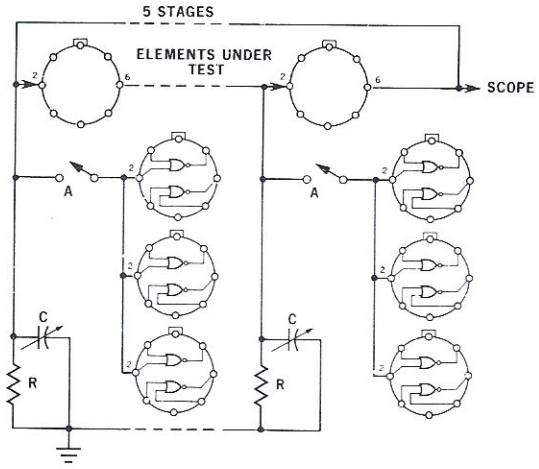


FIG. 11 TEST CIRCUIT AND TABLE FOR TYPICAL t_{pd} MEASUREMENTS



Connect pin 8 to V_{CC}
Connect pin 4 to ground.
Connect all unused input pins to ground

$$\text{AVERAGE } t_{pd} = \frac{1}{f_{osc}} \times \frac{1}{10}$$

ELEMENT	R	INPUT PIN NO.	OUTPUT PIN NO.	OTHER INPUTS	NOTE
908 ADDER	∞	3	7	PINS 2 & 5 TO 1.8 V	2
909 BUFFER	220 Ω	3	6	—	1
910 DUAL GATE	∞	1	7	2, 3, & 5 TO GND	2
912 HALF ADDER	∞	2	6	PIN 3 TO 1.8 V	2

TEST FOR 909 ELEMENTS

1. All "A" switches left open in t_{pd} test for 909 element.
2. For curves shown, fan-out = 1 corresponds to switch "A" open; and for fan-out = 4, switch "A" closed.

AVERAGE PROPAGATION DELAY VERSUS CAPACITANCE

FIG. 12

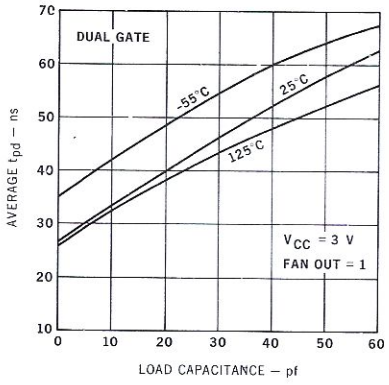


FIG. 13

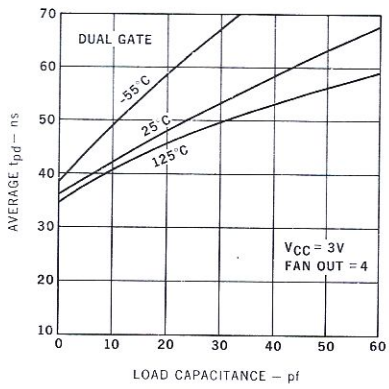


FIG. 14

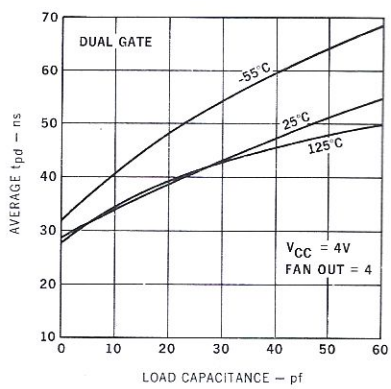


FIG. 15

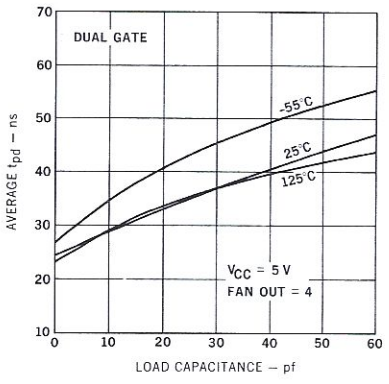


FIG. 16

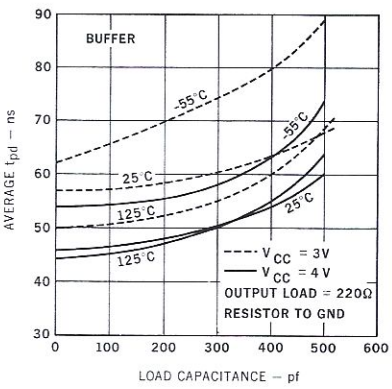
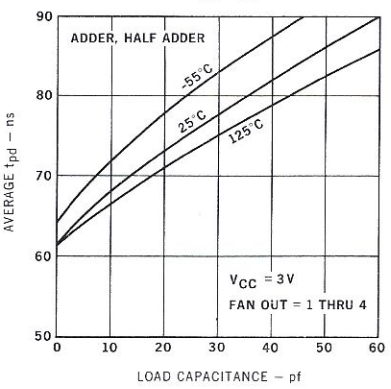


FIG. 17



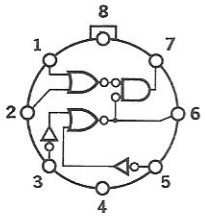
908 MWμL ADDER

THE MWμL ADDER PERFORMS THE **MOD 2** ADDITION OR EXCLUSIVE **OR** FUNCTION; IT ALSO IS USED TO SELECT ONE OF TWO DATA STREAMS UNDER CONTROL OF A SINGLE GATE SIGNAL.

AVERAGE POWER DISSIPATION (25°C)
10 mW

LOGIC SYMBOL AND FUNCTIONS

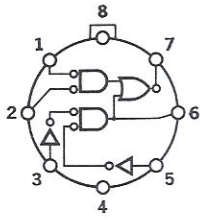
POSITIVE LOGIC



$6 = \overline{(\bar{3}+\bar{5})} = 3 \cdot 5$

$7 = (1+2)\ (\bar{3}+\bar{5})$

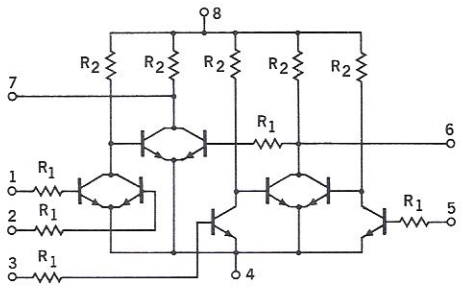
NEGATIVE LOGIC



$6 = \overline{(\bar{3} \cdot \bar{5})} = 3+5$

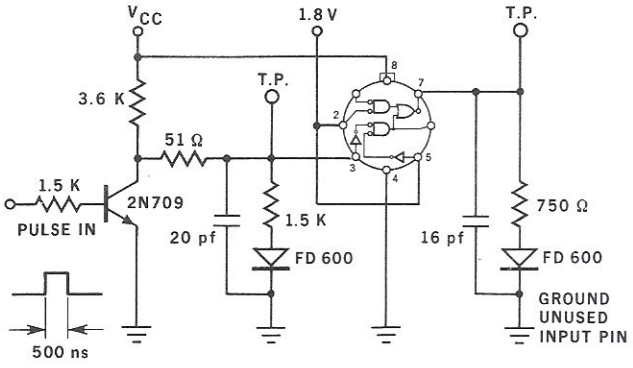
$7 = 1 \cdot 2 + \bar{3} \cdot \bar{5}$

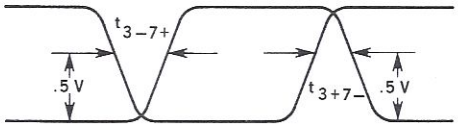
CIRCUIT DIAGRAM



Typical Resistors
$R_1 = 1.5K$
$R_2 = 3.6K$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_3		GND	GND	V_{IN}	GND	GND			V_{CC}		.8 I_{IN}
2	I_5		GND	GND	GND	GND	V_{IN}			V_{CC}		.8 I_{IN}
3	I_1		V_{IN}	V_{BOT}	GND	GND	GND			V_{CC}		I_{IN}
4	I_2		V_{BOT}	V_{IN}	GND	GND	GND			V_{CC}		I_{IN}
5	I_6		GND	GND	V_{ON}	GND	V_{ON}	V_{IN}		V_{CC}	I_{A3}	
6	I_7		V_{ON}	GND	V_{OFF}	GND	V_{OFF}		V_{IN}	V_{CC}	I_{A4}	
7	I_7		GND	V_{ON}	V_{OFF}	GND	V_{OFF}		V_{IN}	V_{CC}	I_{A4}	
8	V_6		GND	GND	V_{BOT}	GND	V_{OFF}			V_{CC}		V_{CE}
9	V_6		GND	GND	V_{OFF}	GND	V_{BOT}			V_{CC}		V_{CE}
10	V_7		V_{OFF}	V_{OFF}	GND	GND	GND			V_{CC}		V_{CE}
11	V_7		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{BOT}	V_{IN}		V_{CC}		V_{CE}
12	V_7		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{BOT}	V_{ON}		V_{CC}		V_{OUT}
13	I_8		GND	GND	GND	GND	GND			V_{LL}		I_L
14	t_{3-7+}		GND	V_{BOT}	Pulse in	GND	V_{BOT}		Pulse out	V_{CC}		80 nsec
15	t_{3+7-}		GND	V_{BOT}	Pulse in	GND	V_{BOT}		Pulse out	V_{CC}		100 nsec

909 MWμL BUFFER

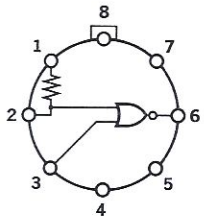
THE MWμL BUFFER IS A LOW IMPEDANCE INVERTING DRIVER CIRCUIT. THE ELEMENT CAN SUPPLY SUBSTANTIALLY MORE OUTPUT CURRENT THAN THE BASIC **RTL** CIRCUIT. A RESISTOR IS INTERNALLY CONNECTED TO THE BUFFER ELEMENT INPUT WHICH MAY BE RETURNED TO THE SUPPLY VOLTAGE IF CAPACITIVE COUPLING IS DESIRED. TYPICAL APPLICATIONS OF THIS TYPE CONNECTION ARE ASTABLE AND MONOSTABLE MULTIVIBRATORS, AND FOR THE DIFFERENTIATION OF PULSES.

AVERAGE POWER DISSIPATION (25°C)

10 mW at 50% Duty Cycle

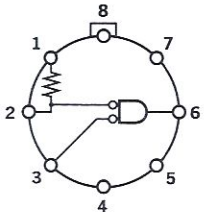
LOGIC SYMBOL AND FUNCTIONS

POSITIVE LOGIC



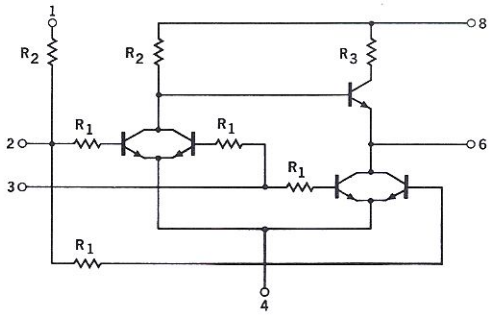
$6 = \overline{2+3}$

NEGATIVE LOGIC



$6 = \overline{2 \cdot 3}$

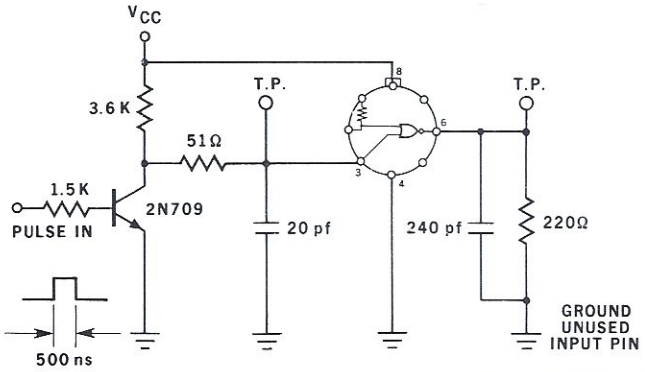
CIRCUIT DIAGRAM

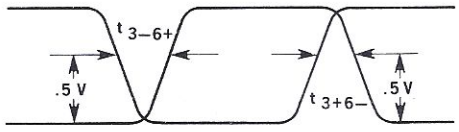


Typical Resistors

$R_1 = 1.5K$
$R_2 = 3.6K$
$R_3 = 100\Omega$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_2			V_{IN}	V_{BOT}	GND				V_{CC}		$2I_{IN}$
2	I_3			V_{BOT}	V_{IN}	GND				V_{CC}		$2I_{IN}$
3	V_6			V_{OFF}	V_{OFF}	GND		V_{IN}		V_{CC}	I_{AB}	
4	V_6			V_{ON}	GND	GND		V_{RH}		V_{CC}		V_{OUT}
5	V_6			GND	V_{ON}	GND		V_{RH}		V_{CC}		V_{OUT}
6	V_6			V_{IN}	GND	GND		V_{RH}		V_{CC}		V_{CE}
7	V_6			GND	V_{IN}	GND		V_{RH}		V_{CC}		V_{CE}
8	I_8			GND	GND	GND				V_{CC}		I_L
9	t_{3+6-}			GND	Pulse in	GND		Pulse out		V_{CC}		90 nsec
10	t_{3-6+}			GND	Pulse in	GND		Pulse out		V_{CC}		70 nsec

910 MWμL DUAL GATE

THE MWμL DUAL GATE MAY BE USED AS A PAIR OF NOR GATES, AS AN R-S FLIP-FLOP, AS A PAIR OF INVERTERS, OR AS A DOUBLE INVERTER. IT MAY ALSO BE USED WITH THE MWμL GATE EXPANDER TO INCREASE ITS FAN-IN CAPACITY.

AVERAGE POWER DISSIPATION (25°C)

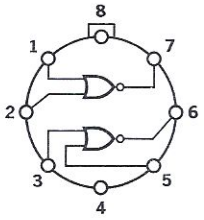
4 mW

LOGIC SYMBOL AND FUNCTIONS

POSITIVE LOGIC

$7 = \overline{1+2}$

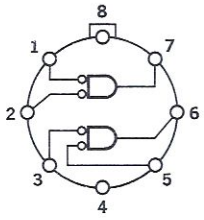
$6 = \overline{3+5}$



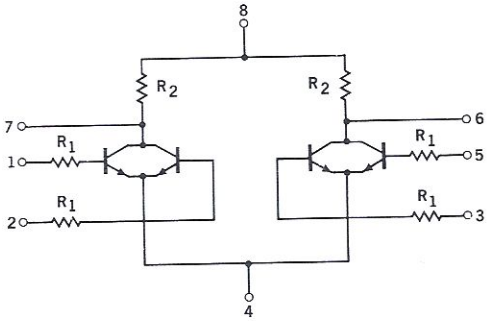
NEGATIVE LOGIC

$7 = \overline{1 \cdot 2}$

$6 = \overline{3 \cdot 5}$



CIRCUIT DIAGRAM

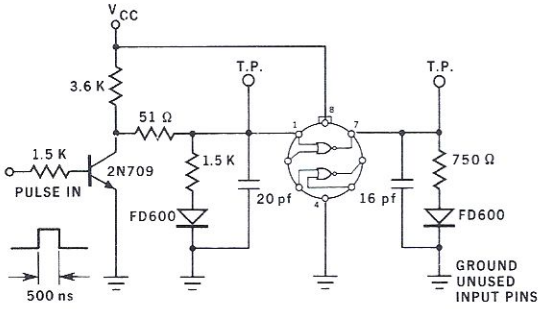


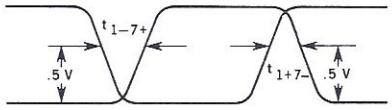
Typical Resistors

$R_1 = 1.5K$

$R_2 = 3.6K$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_1		V_{IN}	V_{BOT}	GND	GND	GND			V_{CC}		I_{IN}
2	I_2		V_{BOT}	V_{IN}	GND	GND	GND			V_{CC}		I_{IN}
3	I_3		GND	GND	V_{IN}	GND	V_{BOT}			V_{CC}		I_{IN}
4	I_5		GND	GND	V_{BOT}	GND	V_{IN}			V_{CC}		I_{IN}
5	I_7		V_{OFF}	V_{OFF}	V_{BOT}	GND	GND		V_{IN}	V_{CC}	I_{A4}	I_{AM}
6	I_6		GND	V_{BOT}	V_{OFF}	GND	V_{OFF}	V_{IN}		V_{CC}	I_{A4}	I_{AM}
7	V_7		V_{ON}	GND	GND	GND	GND			V_{CC}		V_{OUT}
8	V_7		GND	V_{ON}	GND	GND	GND			V_{CC}		V_{OUT}
9	V_6		GND	GND	V_{ON}	GND	GND			V_{CC}		V_{OUT}
10	V_5		GND	GND	GND	GND	V_{ON}			V_{CC}		V_{OUT}
11	V_6		GND	GND	V_{IN}	GND	GND			V_{CC}		V_{CE}
12	V_6		GND	GND	GND	GND	V_{IN}			V_{CC}		V_{CE}
13	V_7		V_{IN}	GND	GND	GND	GND			V_{CC}		V_{CE}
14	V_7		GND	V_{IN}	GND	GND	GND			V_{CC}		V_{CE}
15	I_8		GND	GND	GND	GND	GND			V_{CC}		I_L
16	t_{1-7+}		Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}		40 nsec
17	t_{1+7-}		Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}		50 nsec

911 MWμL GATE

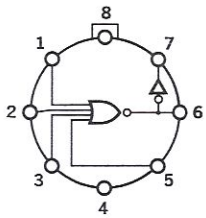
THE MWμL GATE MAY BE USED AS AN **OR** GATE BY APPLYING TRUE INPUTS; THE PIN 7 OUTPUT IS THEN THE TRUE **OR** FUNCTION OF THE INPUTS, AND THE PIN 6 OUTPUT IS THE INVERSE, OR **NOR.**

AVERAGE POWER DISSIPATION (25°C)

4 mW

LOGIC SYMBOL AND FUNCTIONS

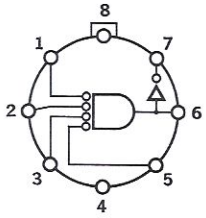
POSITIVE LOGIC



$7 = 1+2+3+5$

$6 = \overline{1+2+3+5}$

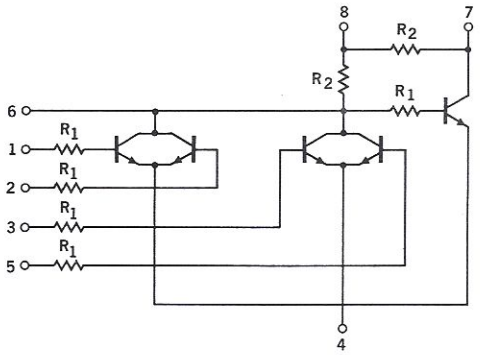
NEGATIVE LOGIC



$7 = 1 \cdot 2 \cdot 3 \cdot 5$

$6 = \overline{1 \cdot 2 \cdot 3 \cdot 5}$

CIRCUIT DIAGRAM

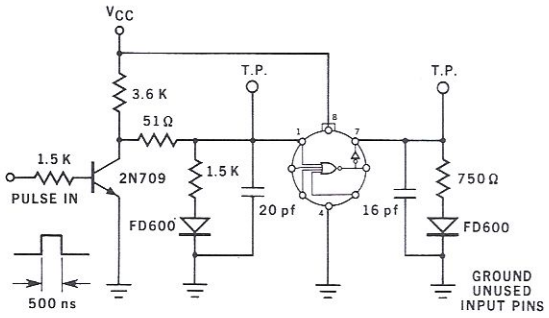


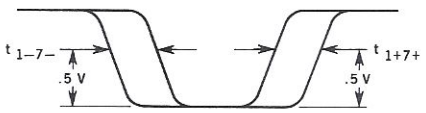
Typical Resistors

$R_1 = 1.5K$

$R_2 = 3.6K$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_1		V_{IN}	V_{BOT}	V_{BOT}	GND	V_{BOT}			V_{CC}		I_{IN}
2	I_2		V_{BOT}	V_{IN}	V_{BOT}	GND	V_{BOT}			V_{CC}		I_{IN}
3	I_3		V_{BOT}	V_{BOT}	V_{IN}	GND	V_{BOT}			V_{CC}		I_{IN}
4	I_5		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{IN}			V_{CC}		I_{IN}
5	I_6		V_{OFF}	V_{OFF}	V_{OFF}	GND	V_{OFF}	V_{IN}		V_{CC}	I_{A3}	
6	I_7		GND	GND	GND	GND	GND	V_{OFF}	V_{IN}	V_{CC}	I_{A4}	I_{AM}
7	V_6		V_{ON}	GND	GND	GND	GND			V_{CC}		V_{OUT}
8	V_6		GND	V_{ON}	GND	GND	GND			V_{CC}		V_{OUT}
9	V_6		GND	GND	V_{ON}	GND	GND			V_{CC}		V_{OUT}
10	V_6		GND	GND	GND	GND	V_{ON}			V_{CC}		V_{OUT}
11	V_6		V_{IN}	GND	GND	GND	GND			V_{CC}		V_{CE}
12	V_6		GND	V_{IN}	GND	GND	GND			V_{CC}		V_{CE}
13	V_6		GND	GND	V_{IN}	GND	GND			V_{CC}		V_{CE}
14	V_6		GND	GND	GND	GND	V_{IN}			V_{CC}		V_{CE}
15	V_7		GND	GND	GND	GND	GND	V_{ON}		V_{CC}		V_{OUT}
16	V_7		GND	GND	GND	GND	GND	V_{IN}		V_{CC}		V_{CE}
17	I_8		GND	GND	GND	GND	GND			V_{LL}		I_L
18	t_{1-7-}		Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}		70 nsec
19	t_{1+7+}		Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}		90 nsec

912 MWμL HALF ADDER

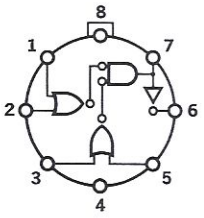
THE MWμL HALF-ADDER IS A MULTI-PURPOSE COMBINATION OF THREE BASIC **RTL** CIRCUITS. THE CONFIGURATION IS WELL SUITED AS A COMPLETE HALF-ADDER, AN EXCLUSIVE **OR** GATE, OR ANY OTHER SIMILAR LOGIC CONSTRUCTION.

AVERAGE POWER DISSIPATION (25°C)

8 mW

LOGIC SYMBOL AND FUNCTIONS

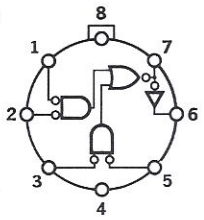
POSITIVE LOGIC



$7 = (1+2)\,(3+5)$

$6 = \bar{1}\cdot\bar{2}+\bar{3}\cdot\bar{5}$

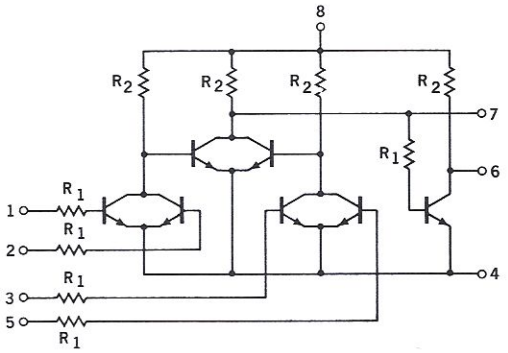
NEGATIVE LOGIC



$7 = 1\cdot2+3\cdot5$

$6 = (\bar{1}+\bar{2})\,(\bar{3}+\bar{5})$

CIRCUIT DIAGRAM

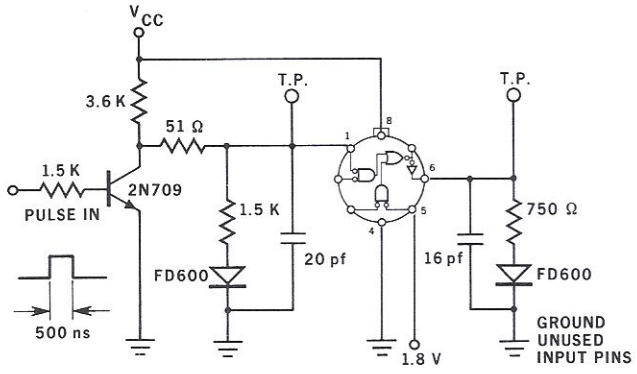


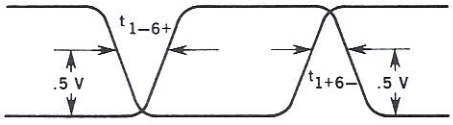
Typical Resistors

$R_1 = 1.5K$

$R_2 = 3.6K$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Notes	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Min.	MAX.
1	I_1		V_{IN}	V_{BOT}	GND	GND	GND			V_{CC}		I_{IN}
2	I_2		V_{BOT}	V_{IN}	GND	GND	GND			V_{CC}		I_{IN}
3	I_3		GND	GND	V_{IN}	GND	V_{BOT}			V_{CC}		I_{IN}
4	I_5		GND	GND	V_{BOT}	GND	V_{IN}			V_{CC}		I_{IN}
5	I_7		V_{ON}	GND	V_{ON}	GND	GND		V_{IN}	V_{CC}	I_{A3}	
6	I_7		GND	V_{ON}	GND	GND	V_{ON}		V_{IN}	V_{CC}	I_{A3}	
7	I_6		GND	GND	GND	GND	GND	V_{IN}		V_{CC}	I_{A4}	
8	V_6		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{BOT}		V_{ON}	V_{CC}		V_{OUT}
9	V_6		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{BOT}		V_{IN}	V_{CC}		V_{CE}
10	V_7		V_{OFF}	V_{OFF}	V_{BOT}	GND	V_{BOT}			V_{CC}		V_{CE}
11	V_7		V_{BOT}	V_{BOT}	V_{OFF}	GND	V_{OFF}			V_{CC}		V_{CE}
12	I_8		GND	GND	GND	GND	GND			V_{LL}		I_L
13	T_{1+6-}		Pulse in	GND	GND	GND	V_{BOT}	Pulse out		V_{CC}		100 nsec
14	T_{1-6+}		Pulse in	GND	GND	GND	V_{BOT}	Pulse out		V_{CC}		80 nsec

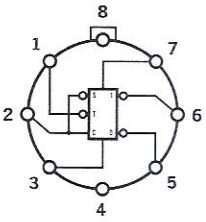
913 MWμL TYPE D FLIP-FLOP

THE MWμL TYPE D FLIP-FLOP IS A COMPLETE, GENERAL PURPOSE STORAGE ELEMENT. THE STATE OF INPUT 2 IS STORED WHEN INPUT 1 CHANGES FROM HIGH TO LOW. A SUBSEQUENT CHANGE OF INPUT 2 WHILE INPUT 1 IS LOW HAS NO EFFECT. THE 913 FLIP-FLOP HAS APPLICATION IN SHIFT REGISTERS, COUNTERS, AND CONTROL CIRCUITRY.

AVERAGE POWER DISSIPATION (25°C)

12 mW

LOGIC SYMBOL AND FUNCTIONS



DIRECT INPUTS[1]

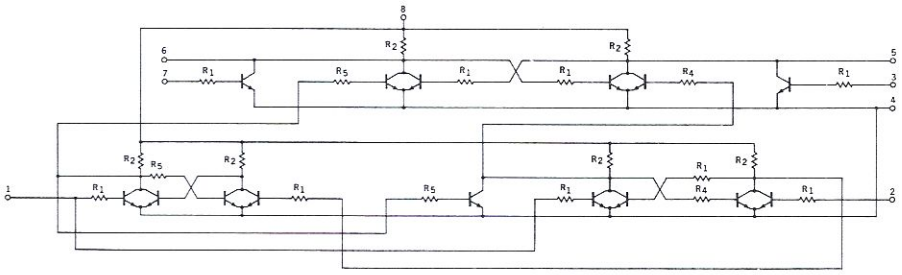
3	7	6	5
L	L	NC	NC[2]
L	H	L	H
H	L	H	L
H	H	L	L

GATED INPUT[3]

t = n	t = n + 1	
2	6	5
H	H	L
L	L	H

1. Pin 1 must be high
2. NC = no change
3. Pins 3 and 7 must be low

CIRCUIT DIAGRAM

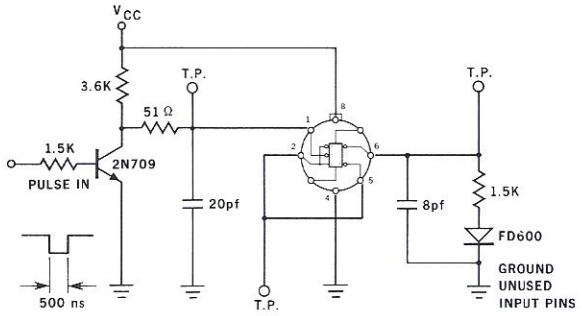


Typical Resistors $R_1 = 1.5K$ $R_4 = 180\Omega$ $R_2 = 3.6K$ $R_5 = 480\Omega$

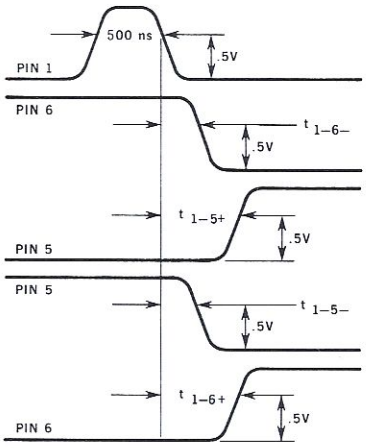
Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	V_5		V_{BOT}	GND	V_{ON}	GND			V_{BOT}	V_{CC}		V_{OUT}
2	V_6		V_{BOT}	GND	V_{BOT}	GND			V_{ON}	V_{CC}		V_{OUT}
3	V_5		V_{BOT}	GND	GND	GND		V_{ON}	GND	V_{CC}		V_{OUT}
4	V_6		V_{BOT}	GND	GND	GND	V_{ON}		GND	V_{CC}		V_{OUT}
5	V_5		V_{BOT}	GND	V_{IN}	GND			V_{BOT}	V_{CC}		V_{CE}
6	V_6		V_{BOT}	GND	V_{BOT}	GND			V_{IN}	V_{CC}		V_{CE}
7	V_5		V_{BOT}	GND	GND	GND		V_{IN}	GND	V_{CC}		V_{CE}
8	V_6		V_{BOT}	GND	GND	GND	V_{IN}		GND	V_{CC}		V_{CE}
9	I_1		V_{IN}	GND	GND	GND			GND	V_{CC}		1.8 I_{IN}
10	I_1		V_{IN}	V_{BOT}	GND	GND			GND	V_{CC}		1.8 I_{IN}
11	I_5		V_{ON}	V_{BOT}	V_{OFF}	GND	V_{IN}		V_{BOT}	V_{CC}	I_{A3}	
12	I_6		V_{ON}	GND	V_{BOT}	GND		V_{IN}	V_{OFF}	V_{CC}	I_{A3}	
13	I_5	1	V_{OFF}	GND	V_{OFF}	GND	V_{IN}		V_{BOT}	V_{CC}	I_{A3}	
14	I_6	1	V_{OFF}	V_{ON}	V_{BOT}	GND		V_{IN}	V_{OFF}	V_{CC}	I_{A3}	
15	I_2	1	V_{OFF}	V_{IN}	GND	GND			GND	V_{CC}		I_{IN}
16	I_3	1	V_{OFF}	V_{BOT}	V_{IN}	GND			GND	V_{CC}		I_{IN}
17	I_7	1	V_{OFF}	GND	GND	GND			V_{IN}	V_{CC}		I_{IN}
18	V_5	1	V_{OFF}	V_{ON}	GND	GND			V_{BOT}	V_{CC}		V_{CE}
19	V_6	1	V_{OFF}	V_{OFF}	V_{BOT}	GND			GND	V_{CC}		V_{CE}
20	I_8		GND	GND	GND	GND			GND	V_{LL}		I_L
21	t_{1-6-}		Pulse In	Tie to Pin 5	GND	GND		Pulse Out	GND	V_{CC}		80 nSec
22	t_{1-6+}		Pulse In	Tie to Pin 5	GND	GND		Pulse Out	GND	V_{CC}		120 nSec
23	t_{1-5-}		Pulse In	Tie to Pin 5	GND	GND	Pulse Out		GND	V_{CC}		80 nSec
24	t_{1-5+}		Pulse In	Tie to Pin 5	GND	GND	Pulse Out		GND	V_{CC}		120 nSec
25	t_{2+1-}		Pulse 1 In	Pulse 2 In	GND	GND		Pulse Out	GND	V_{CC}	60 nSec	
26	t_{1-2-}		Pulse 1 In	Pulse 2 In	GND	GND		Pulse Out	GND	V_{CC}	30 nSec	
27	t_{2-1-}		Pulse 1 In	Pulse 2 In	GND	GND		Pulse Out	GND	V_{CC}	60 nSec	
28	t_{1-2+}		Pulse 1 In	Pulse 2 In	GND	GND		Pulse Out	GND	V_{CC}	30 nSec	

Note 1: Voltage applied to Pin 1 changes from V_{RL} to specified value prior to making measurements.

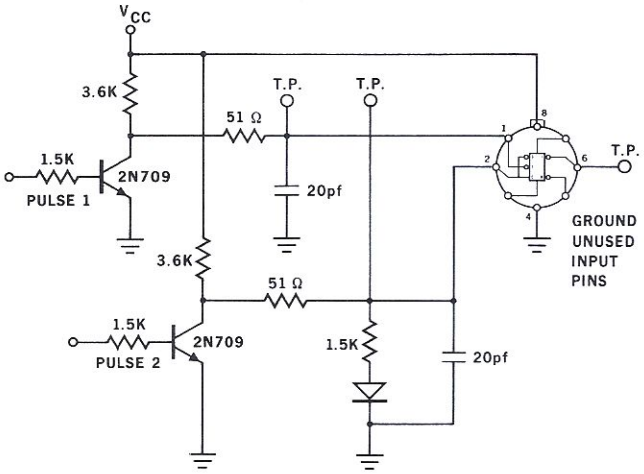
CIRCUIT FOR MEASURING T_{I-6+}, T_{I-6-}, T_{I-5+}, T_{I-5-}



PROPAGATION DELAY

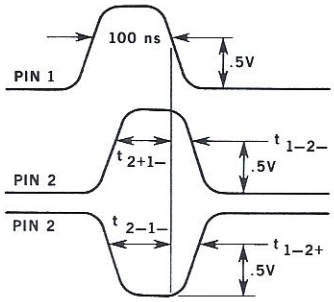


CIRCUIT FOR MEASURING MINIMUM INPUT PULSE WIDTH

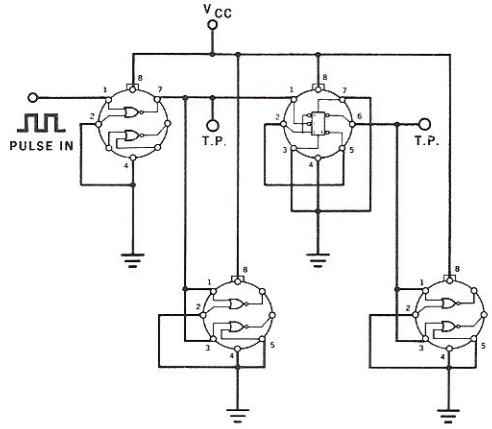


VARIABLE DELAY BETWEEN PULSE 1 AND PULSE 2

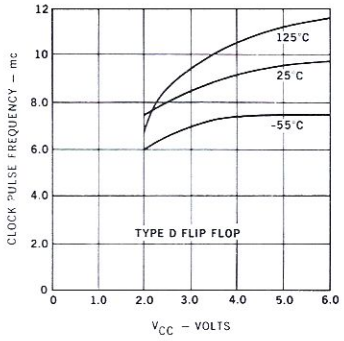
MINIMUM PULSE WIDTH

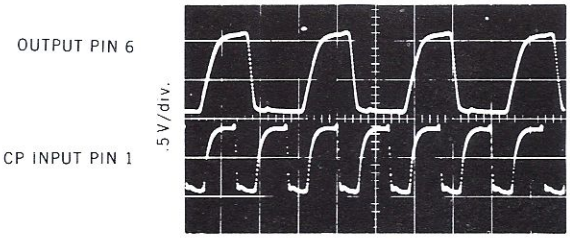


CONNECTED AS BINARY COUNTER



TYPICAL OPERATING CLOCK PULSE FREQUENCY VERSUS V_{CC}





100 nsec/div.

921 MWμL GATE EXPANDER

THE MWμL GATE EXPANDER IS A DOUBLE GATE WITHOUT THE NODE RESISTORS. ITS OUTPUT TERMINALS MAY BE CONNECTED IN PARALLEL TO THOSE OF A DUAL GATE OR A GATE TO INCREASE THE FAN-IN CAPABILITY OF THE CIRCUITS.

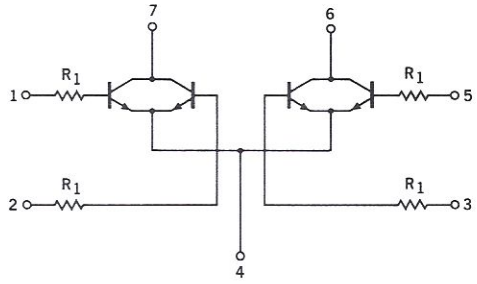
WHEN A DUAL GATE OR A GATE IS USED WITH THE EXPANDER, THE FOLLOWING RULES APPLY.

1) Pin 8 of the Expander must be connected to V_{CC}
2) The input load factor of the expanded gate is 1.33
3) The output drive factor of the expanded gate is decreased by .5 load for every node added.

AVERAGE POWER DISSIPATION (25°C)

No Power Flowing

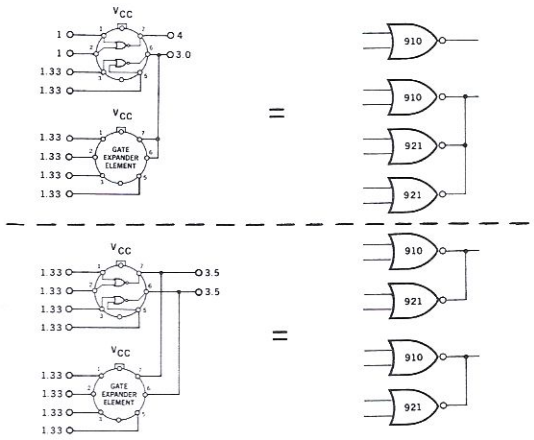
CIRCUIT DIAGRAM



Typical Resistor

$R_1 = 1.5K$

DIAGRAM FOR USE OF GATE EXPANDER



Example of loading rules and logic symbols

Test No.	Test	Notes	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_1		V_{IN}	V_{BOT}	GND	GND	GND		V_{RH}	V_{CC}		I_{IN}
2	I_2		V_{BOT}	V_{IN}	GND	GND	GND		V_{RH}	V_{CC}		I_{IN}
3	I_3		GND	GND	V_{IN}	GND	V_{BOT}	V_{RH}		V_{CC}		I_{IN}
4	I_5		GND	GND	V_{BOT}	GND	V_{IN}	V_{RH}		V_{CC}		I_{IN}
5	V_7		V_{ON}	GND	GND	GND	GND		V_{RL}	V_{CC}		V_{OUT}
6	V_7		GND	V_{ON}	GND	GND	GND		V_{RL}	V_{CC}		V_{OUT}
7	V_6		GND	GND	V_{ON}	GND	GND	V_{RL}		V_{CC}		V_{OUT}
8	V_6		GND	GND	GND	GND	V_{ON}	V_{RL}		V_{CC}		V_{OUT}
9	V_6		GND	GND	V_{IN}	GND	GND	V_{RL}		V_{CC}		V_{CE}
10	V_6		GND	GND	GND	GND	V_{IN}	V_{RL}		V_{CC}		V_{CE}
11	V_7		V_{IN}	GND	GND	GND	GND		V_{RL}	V_{CC}		V_{CE}
12	V_7		GND	V_{IN}	GND	GND	GND		V_{RL}	V_{CC}		V_{CE}
13	I_7		V_{OFF}	V_{OFF}	GND	GND	GND		V_{IN}	V_{CC}		I_{CEX}
14	I_6		GND	GND	V_{OFF}	GND	V_{OFF}	V_{IN}		V_{CC}		I_{CEX}
15	$I_{6,7,8}$		GND	GND	GND	GND	GND	V_{CC}	V_{CC}	V_{CC}		I_L

FAIRCHILD ASSURED CUSTOMER TEST PROGRAM

Note to Buyers: This document is a complete procurement specification which can be referred to as a purchase contract.

1.0 SCOPE

This specification covers detailed requirements for high reliability planar-epitaxial micrologic devices suitable for use in space vehicles and under extreme environmental conditions.

2.0 FAILURE RATES

2.1 While the acceptance conditions for operation life, storage life, and environmental tests are assured by actual test, the estimated failure rate in conservatively designed equipment is a figure arrived at by engineering judgment and relationship to devices actually tested by Fairchild which have been shown to have a failure rate of .02% per thousand hours. The vendor is not required to demonstrate this failure rate on devices shipped.

3.0 APPLICABLE DOCUMENTS

3.1 Testing Procedures — Test procedures shall conform to MIL-M-23700 or MIL-S-19500 and MIL-STD-750.

3.2 Sampling Procedures — Sampling procedures used are per MIL-M-23700 or MIL-S-19500, unless otherwise specified.

4.0 MISCELLANEOUS REQUIREMENTS

4.1 Packaging — Devices shall be packed in the vendor's standard package unless otherwise specified on the purchase order.

5.0 QUALITY AND RELIABILITY ASSURANCE PROVISIONS

5.1 100% Processing Steps — Processing steps to eliminate early failures are described in Table II.

5.2 Normal Lot Acceptance — Each lot of devices shipped shall meet the requirements of Table I - Group A Inspection and shall be accompanied by variables data on the latest completed lot of continuous production submitted to Table III - Group B Inspection.

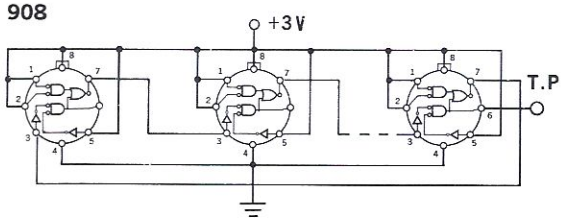
6.0 DEFINITIONS

6.1 LTPD (Lot Tolerance Percent Defective) — This parameter of a sampling plan is the maximum percent defective which will be accepted by the sampling plan with 90% confidence.

OPERATING LIFE TEST

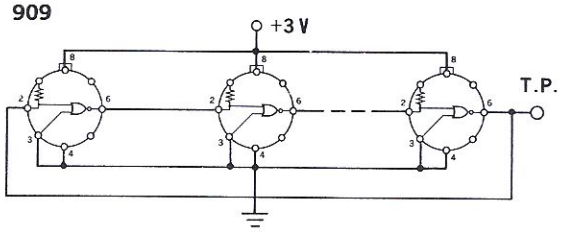
The rings are operated at +125°C. Ninety-five percent of the power in MWμL systems is dissipated in the resistors. These rings cause every resistor to dissipate its normal power and therefore stress each element at its maximum operating temperature.

908



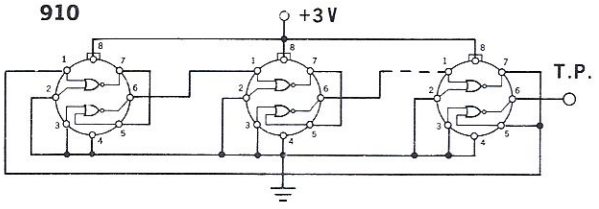
ODD NO. OF UNITS

909



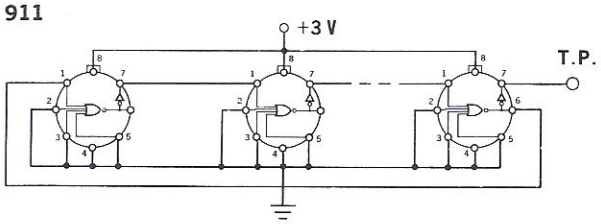
ODD NO. OF UNITS

910



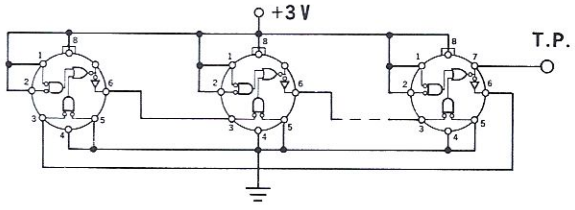
ANY NO. OF UNITS

911



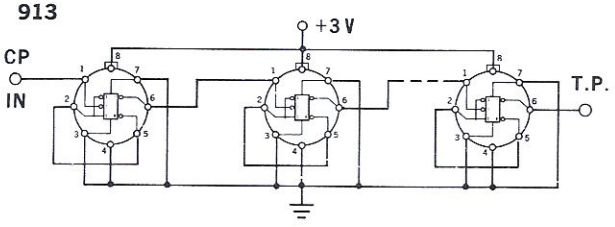
ANY NO. OF UNITS

912



ODD NO. OF UNITS

913



$f_{cp} \leq 1mc$

FAIRCHILD ASSURED CUSTOMER TEST PROGRAM

TABLE I — GROUP A INSPECTION — L.T.P.D.

ELEMENT	TEST #		25°C	−55°C	+125°C
908	1, 2, 3, 4	Combined	10%	15%	15%
	5, 6, 7	Combined	10%	15%	15%
	8, 9, 10, 11, 12	Combined	10%	15%	15%
	13		5%	—	10%
	14, 15	Combined	10%	—	—
909	1, 2	Combined	10%	15%	15%
	3		10%	15%	15%
	4, 5	Combined	10%	15%	15%
	6, 7	Combined	10%	15%	15%
	8		5%	—	10%
	9, 10	Combined	10%	—	—
910	1, 2, 3, 4	Combined	10%	15%	15%
	5, 6	Combined	10%	15%	15%
	7, 8, 9, 10	Combined	10%	15%	15%
	11, 12, 13, 14	Combined	10%	15%	15%
	15		5%	—	10%
	16, 17	Combined	10%	—	—
911	1, 2, 3, 4	Combined	10%	15%	15%
	5, 6	Combined	10%	15%	15%
	7, 8, 9, 10, 15	Combined	10%	15%	15%
	11, 12, 13, 14, 16	Combined	10%	15%	15%
	17		5%	—	10%
	18, 19	Combined	10%	—	—
912	1, 2, 3, 4	Combined	10%	15%	15%
	5, 6, 7	Combined	10%	15%	15%
	8		10%	15%	15%
	9, 10, 11	Combined	10%	15%	15%
	12		5%	—	10%
	13, 14	Combined	10%	—	—
913	1, 2, 3, 4	Combined	10%	15%	15%
	5, 6, 7, 8	Combined	10%	15%	15%
	9, 10, 15, 16, 17	Combined	10%	15%	15%
	11, 12, 13, 14	Combined	10%	15%	15%
	18, 19	Combined	10%	15%	15%
	20		5%	—	10%
	21,22, 23, 24, 25, 26, 27, 28	Combined	10%	—	—
921	1, 2, 3, 4	Combined	10%	15%	15%
	5, 6, 7, 8	Combined	10%	15%	15%
	9, 10, 11, 12	Combined	10%	15%	15%
	13, 14, 15	Combined	5%	—	10%

TABLE II — 100% PROCESSING

Test No.	MIL-STD-750 Ref. Para.	Examination or Test	Conditions (T_A = 25°C unless otherwise specified)
1	1052	Temperature Cycling	3 cycles −65°C to +200°C
2	—	High .mpact Shock *	25,000 g (min)
		(Y_1 axis only)	Pulse Width = 20μsec (min)
3	—	Fine Hermetic Seal Leak Test (Radiflo)	10^{-5}cc/sec (max)

* Constant Acceleration, Y_1 axis only, at 20,000 g may be substituted for this test at the vendor's option.

TABLE III — GROUP B INSPECTION

Test No.	MIL-STD-750 Ref. Para.	Examination or Test	Conditions (T_A = 25°C unless otherwise specified)	Sample Size	Accept No.
		SUBGROUP I			
1	1026	Operating Life (1000 hours)	V_{CC} = 3 Vdc, T_A = 125°C (in-ring counter circuit)	30	1 †
2	2016	Shock Test	3000 g, 0.2 msec, 5 blows in each of 6 orientations		
3	2046	Vibration Fatigue	20 g, 40 cps, 96 hours, 3 orientations		
4	2056	Vibration, Variable Frequency	100-2000-100 cps, 20 g peak acceleration, 3 orientations		
5	2006	Constant Acceleration	40,000 g, 2 orientations		
6	1056	Thermal Shock	−65°C to +125°C, 5 cycles		
7	1052	Temperature Cycling	−65°C to +200°C, 10 cycles ½ hr. at each temp. extreme per cycle.		
8	1021	Moisture Resistance	MIL-STD-202B Method 106A		
		END POINTS (T_A = 25°C)*			

	908	909	910	911	912	913	921
Test #	1	1	1	1	1	1	1
	5	5	5	5	5	6	5
	8	6	9	7	8	9	9
	12	8	14	11	9	11	15
4 tests/element							

* Limits for Group B Inspection are identical to Group A limits for the same test.

		SUBGROUP II			
1	2016	Shock Test	3000 g, 0.2 msec, 5 blows in each of 6 orientations	25	1 †
2	2046	Vibration Fatigue	20 g, 40 cps, 96 hours, 3 orientations		
3	2056	Vibration, Variable Frequency	100-2000-100 cps, 20 g peak acceleration, 3 orientations		
4	2006	Constant Acceleration	40,000 g, 2 orientations		
5	1056	Thermal Shock	−65°C to +125°C, 5 cycles		
6	1052	Temperature Cycling	−65°C to +200°C, 10 cycles ½ hr. at each temp. extreme per cycle		
7	1021	Moisture Resistance	MIL-STD-202B Method 106A		
8	1031	Storage Life 1000 hours	150°C		
		END POINTS Same as for Subgroup 1			
		SUBGROUP III			
1	1041	Salt Atmosphere	END POINTS—No Illegible Markings or Destructive Corrosion	10	1
		SUBGROUP IV			
	2036-E	Lead Fatigue	END POINTS—Failure If One or More Leads Break	10	1
		SUBGROUP V			
1	2026	Solderability	END POINTS—Per Method 208 MIL-STD-202 (No Electrical End Points Are Applicable)	10	1

† Acceptance number applies to Readout of End Points immediately after test 1 of subgroup I and test 7 of subgroup II. Other tests in these subgroups are for information only.

MILLIWATT MICROLOGIC (MWμL) SYMBOLS AND DEFINITIONS

V_{CC}	Supply Voltage
V_{LL}	A d-c Voltage low enough that only leakage currents flow from the supply terminal. It is used for leakage test on Gates, Type D Flip-Flops, Adders, and Half-Adders.
V_{BOT}	The Maximum Input Voltage encountered in a MWμL system.
V_{IN}	Minimum High level encountered in a MWμL system.
V_{ON}	Maximum Voltage required to turn on a transistor.
V_{OFF}	The Maximum Voltage which may be applied to an input terminal without turning on the transistor.
V_{OUT}	The Output Voltage when V_{ON} is applied to the input pin.
V_{CE}	The Output Voltage when V_{IN} is applied to the input pin.
I_{A4}	Current available from an output terminal with a fan-out of −4.
I_{A3}	Current available from an output terminal with a fan-out of −3.
I_{AB}	Current available from the output terminal of a Buffer.
I_{AM}	Maximum Current available from the output terminal of a Gate of a Dual Gate.
I_{IN}	The current drawn from the V_{IN} supply by one input of a gate with a fan-in of two or more.
$.8I_{IN}$	The current drawn from the V_{IN} supply by the input of a MWμL inverter or a gate with fan-in = 1.
$1.8I_{IN}$	The current drawn from the V_{IN} supply by a Type D Flip-Flop clock pulse input terminal, Pin 1.
$2\ I_{IN}$	The current drawn from the V_{IN} supply by a Buffer element input terminal
I_{CEX}	Collector current of Gate Expander when V_{OFF} is applied to the input pins and V_{IN} applied to the output pin.
I_L	Leakage current.
V_{RL}	Voltage Drop obtained through a resistor to V_{CC}. This resistor represents the lowest node resistor of MWμL circuit.
V_{RH}	Voltage Drop obtained through a resistor to V_{CC}. This resistor represents the highest node resistor of MWμL circuit.

MWμL SYMBOLS AND TEST LIMITS

		−55°C	+25°C	+125°C
V_{CC}	(V)	3.00 ±.01	3.00 ±.01	3.00 ±.01
V_{LL}	(mV)	500 ±2	400 ±2	300 ±2
V_{BOT}	(V)	1.80 ±.01	1.80 ±.01	1.80 ±.01
V_{IN}	(mV)	970 ±2	805 ±2	590 ±2
V_{ON}	(mV)	935 ±2	750 ±	555 ±2
V_{OFF}	(mV)	650 ±2	450 ±	260 ±
V_{OUT}	(mV)	620	300	230
V_{CE}	(mV)	220	220	220
I_{A4}	(μA)	475	494	418
I_{A3}	(μA)	350	364	308
I_{AB}	(mA)	3.75	4.0	3.3
I_{AM}	(μA)	730	815	830
I_{IN}	(μA)	125	130	110
I_{CEX}	(μA)	5	5	40
I_L	(μA)	100	100	100
V_{RL}*		2.8 K ±1%	2.7 K ±1%	3 K ±1%
V_{RH}*		4.27 K ±1%	4.3 K ±1%	5 K ±1%

* Resistor to V_{CC}

IMPROVED OPERATION AT $V_{CC} = 4$ V

The typical curves on earlier pages show greatly improved fan-out-noise immunity relationships as well as improved speed at $V_{CC} = 4$ V. The following tables give suggested specification numbers for operation at $V_{CC} = 4$ V with fan-out 4 and improved noise margin specifications or fan-out 5 and the same margins. These numbers are based on conservative correlations to the table on page 20 which is verified by QA sampling.

At 4 V V_{CC} the increased power drain in the units is often overcome by improved power supply efficiency. Note also that units from the same distributions have improved thresholds to ground noise in the fan-out = 5 at 4 V even though the specified noise margin is the same as the fan-out = 4 case at 3 Volt V_{CC}.

		$V_{CC} = 4$ V F.O. = 4 N.I. = 60 mV			**$V_{CC} = 4$ V F.O. = 5 N.I. = 30 mV**		
SYMBOL	UNITS	−55°C	+25°C	+125°C	−55°C	+25°C	+125°C
V_{CC}	(V)	4.00 V	4.00 V	4.00 V	4.00 V	4.00 V	4.00 V
V_{LL}	(mV)	500	400	300	500	400	300
V_{BOT}	(V)	2.0	2.0	2.0	2.0	2.0	2.0
V_{IN}	(mV)	1035	865	660	1000	825	625
V_{CE}	(mV)	240	240	210	240	240	220
V_{ON}	(mV)	975	775	600	970	775	595
V_{OUT}	(mV)	580	300	220	620	300	230
V_{OFF}	(mV)	650	450	280	650	450	260
I_{A4}	μa	685	720	620	700	730	630
I_{A3}	μa	515	540	465	560	584	504
I_{IN}	μa	180	180	163	146	146	131
I_{AB}	ma	5.0	5.34	4.4	5.0	5.34	4.4
I_{AM}	ma	1.050	1.150	1.050	1.050	1.160	1.075
I_{CEX}	μa	5	10	75	5	5	40
I_L	μa	100	100	100	100	100	100
V_{RL}		2.8 K	2.7 K	3 K	2.8 K	2.7 K	3 K
V_{RH}		4.27 K	4.3 K	5 K	4.27 K	4.3 K	5 K

LOADING RULES FOR MIXED MWμL AND μL SYSTEMS (3V, V_{CC})

Rules

A MWμL Fan-Out 3 node cannot drive a μL input.

A MWμL Fan-Out 4 node can drive one μL unit input load only.

A MWμL Buffer (909) will have 28 MWμL unit loads available when driving a combination of MWμL and μL; each MWμL unit input load will require 1.6 loads when in parallel with μL and each μL unit input load will require 4.3 MWμL loads when in parallel with MWμL. A MWμL Buffer (909) when driving **only** μL inputs can drive 7 μL unit input loads.

A μL Buffer (900, 928) has 25 μL loads available when driving mixed μL and MWμL inputs, with each μL unit input load requiring 1.0 loads and each MWμL unit input load requiring 0.4 μL loads. The μL Buffer driving MWμL inputs **only** can drive 100 MWμL unit loads.

A μL Fan-Out 5 node can drive 5 loads of mixed μL and MWμL. Each μL input = 1.0 loads and each MWμL input = 0.4 loads. A μL Fan-Out 5 node driving MWμL inputs **only** can drive 20 MWμL unit loads.

A μL Fan-Out 4 node can drive 4 loads of mixed μL and MWμL. Each μL input = 1.0 loads and each MWμL input = 0.4 loads.

A μL Fan-Out 3 node can drive 3 loads of mixed μl and MWμL. Each μL input = 1.0 loads and each MWμL input = 0.4 loads.

These rules apply to operation at $V_{CC} = 3$ V and −55°C to +100°C for μL outputs driving MWμL inputs except that μL Buffers (900, 928) may be used to +125°C. MWμL outputs may drive μL inputs through the full −55°C to +125°C temperature range.

FAIRCHILD

SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

Fairchild cannot assume responsibility for use of any circuitry described. No circuit patent licenses are implied.